HPC-architectures

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Instruction level parallelism = ILP

First universal ILP: pipelining (since 1985)

- Two approaches to ILP

Discover and exploit **parallelism in hardware**

(Dominant in server and desktop market segments; Not used in PMD segment due to energy constraints)

Software-based discovery at compile time

(Technical markets, scientific computing, HPC)

Instruction Parallelism Examples

- Loop-level parallelism
  - Loop unrolling (compiler)
  - Dynamic unrolling (superscalar scheduling)
- Data parallelism
  - Vector computers
    - Cray X1, X1E, X2; NEC SX-9
  - SIMT
    - GPUs
  - SIMD
    - Short SIMD (SSE, AVX, Intel Phi)